

## MPC7450

# High Performance, Low-Power 32-Bit PowerPC™ RISC Microprocessor

The MPC7450 PowerPC microprocessor is a high-performance, low-power, 32-bit implementation of the PowerPC RISC architecture with a full 128-bit implementation of Motorola's AltiVec technology. This microprocessor is ideal for leading-edge computing, embedded network control, and signal processing applications. The MPC7450 has a new, deeper, seven-stage pipeline with two additional execution units. The L2 cache has been integrated onto the die for greater speed, and supports a large backside L3 cache with a 64-bit datapath. The MPC7450 offers increased address space and high-bandwidth MPX bus with minimized signal setup times and reduced idle cycles to increase bus bandwidth to a maximum speed of 133 MHz. MPC7450 processors offer single-cycle throughput double precision floating-point performance and full symmetric multi-processing (SMP) capabilities. Finally, the

MPC7450 is software-compatible with existing PowerPC 603e, 750, 7400 and 7410 processors and exploits the full potential of AltiVec technology.

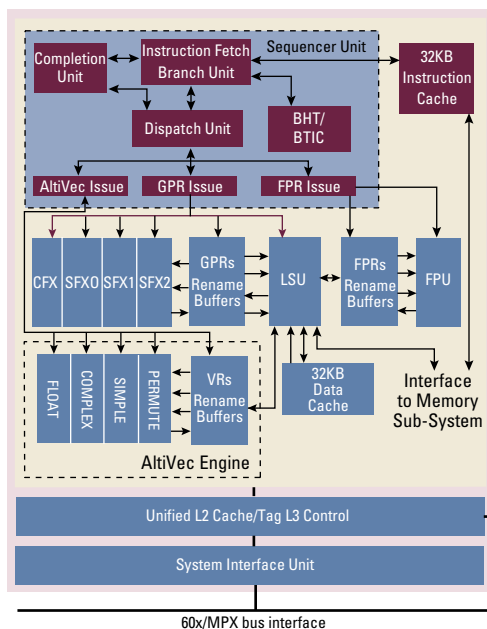
## Superscalar Microprocessor

MPC7450 microprocessors feature a high-frequency superscalar PowerPC core, capable of issuing four instructions per clock cycle (three instructions + branch) into eleven independent execution units:

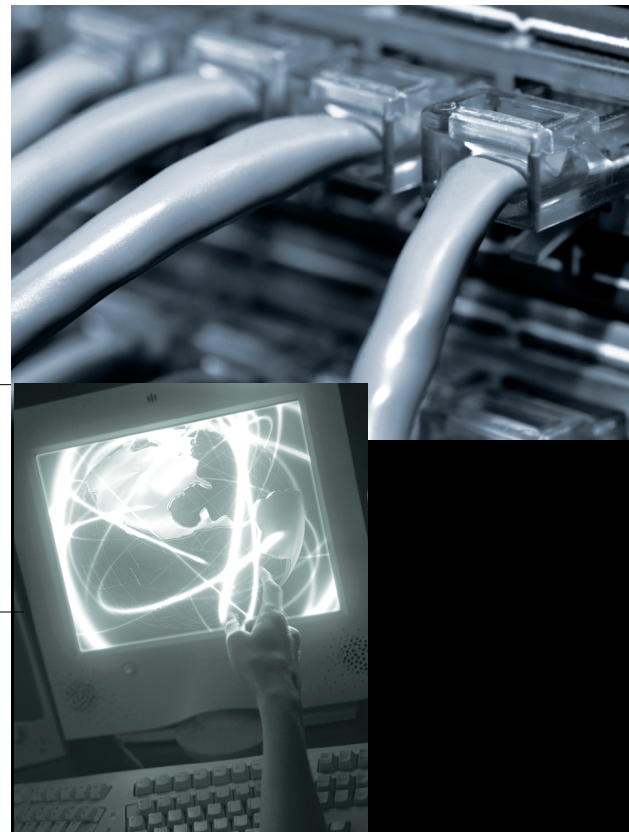
- Four integer units (3 simple + 1 complex)
- Double-precision floating-point unit
- Four AltiVec units (simple, complex, floating, and permute)
- Load/store unit
- Branch processing unit

## Cache and MMU Support

The MPC7450 microprocessor has separate 32KB, physically addressed instruction and data caches. Both L1 caches feature cache way locking and are eight-way set associative. For greater speed, the L2 cache has been integrated on-chip with a 256-bit interface to L1 which operates at processor frequency. This L2 is 256KB eight-way set associative. L2 cache access is fully pipelined. The MPC7450 also supports an L3 cache interface with on-chip tags to support up to 2MB of off-chip cache. The L3 data bus is 64-bits wide, provides multiple SRAM



MPC7450 Block Diagram



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	MPC7450
<b>CPU Speeds – Internal</b>	533, 667 and 733 MHz
<b>Bus Frequency</b>	133 MHz
<b>Bus Interface</b>	64-bit
<b>Bus Protocol</b>	MPX/60x
<b>Instructions per Clock</b>	4 (3 + Branch)
<b>Integrated L1 Cache</b>	32 KB instruction 32 KB data
<b>Integrated L2 Cache</b>	256 KB
<b>L3 Cache</b>	1 or 2 MB
<b>Typical/Maximum Power Dissipation</b>	14W /17W @ 533 MHz
<b>Die Size</b>	106 mm <sup>2</sup>
<b>Package</b>	483 CBGA
<b>Process</b>	0.18µ 6LM CMOS
<b>Voltage</b>	1.8V internal, 1.8/2.5V I/O
<b>SPECint95 (estimated)</b>	32.1 @ 733 MHz
<b>SPECfp95 (estimated)</b>	23.9 @ 733 Mhz
<b>Other Performance</b>	1324 Drystone 2.1 MIPS @ 733 MHz
<b>Execution Units</b>	Integer(4), Floating-Point, AltiVec(4), Branch, Load/Store

## Contact Information

Motorola offers user's manuals, application notes, sample code and full local support for the PowerPC product line. For more information, visit:

<http://motorola.com/PowerPC/> and  
<http://motorola.com/AltiVec/>

For all other inquiries about Motorola products, please contact the Motorola Customer Response Center at: 1-800-521-6274 or

<http://motorola.com/semiconductors>

options, and affords critical quad-word forwarding to reduce latency. The off-chip L3 storage can also be configured as a local addressable memory. Finally, in addition to supporting hardware table searching on a TLB miss, the MPC7450 can be configured for software table searching. In this case, TLB entries are loaded by the system software.

The MPC7450 microprocessor contains separate memory management units for instructions and data, supporting 4 Petabytes (2<sup>52</sup>) of virtual memory and up to 64 Gigabytes (2<sup>36</sup>) of physical memory. The MPC7450 also has four instruction block address translation and four data block address translation registers.

## MPX Bus Interface

MPC7450 microprocessors support the MPX bus protocol with a 64-bit data bus and a 32- or 36-bit address bus. Support is included for burst, split, pipelined and out-of-order transactions, in addition to data streaming, and data intervention (in SMP systems). The interface provides snooping for data cache coherency. The MPC7450 implements the cache coherency protocol for multiprocessing support in hardware, allowing access to system memory for additional caching bus masters, such as DMA devices.

## Power Management

MPC7450 microprocessors feature a low-power 1.8-volt design with three power-saving user-programmable modes – nap, doze (with bus snoop) and sleep – which progressively

reduce the power drawn by the processor. The MPC7450 also provides a thermal assist unit and instruction cache throttling for software-controllable thermal management.

## AltiVec Technology

The AltiVec technology expands the capabilities of Motorola's fourth generation PowerPC microprocessors by providing leading-edge, general purpose processing performance while concurrently addressing high-bandwidth data processing and algorithmic-intensive computations in a single-chip solution. AltiVec technology:

- Meets the computational demands of networking infrastructure such as echo cancellation equipment, and basestation processing.
- Enables faster, more secure encryption methods optimized for the SIMD processing model.
- Provides compelling performance for multimedia-oriented desktop computers, desktop publishing, and digital video processing.
- Enables real-time processing of the most demanding data streams (MPEG-2 encode, continuous speech recognition, real-time high-resolution 3D memory for 3D graphics.)



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